CPTO

26 OCT 04

RJT

CLAIMS 1-12 CANCELED

13. (Amended) A method of fabricating a semiconductor device comprising a silicon substrate carrying a ground plane, a dielectric layer provided on said ground plane, a signal layer provided on said dielectric layer, a depression formed in said dielectric layer so as to extend down to said substrate through said signal layer and said ground plane, and a semiconductor chip carrying thereon an air bridge structure, said semiconductor chip being flip chip mounted onto said silicon substrate, said method comprising the steps of:

forming said depression in said silicon substrate by an etching process; and

mounting said semiconductor chip on said silicon substrate such that said air bridge structure is accommodated into said depression.

14. (Amended) A method as claimed in claim 13, wherein said etching step includes a wet etching process applied to said silicon substrate.

CLAIM 15 CANCELED